

: 10/591173

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IAP5 Rec'd PCT/PTO 30 AUG 2006

## SPECIFICATION

## TITLE OF THE INVENTION

5 HIGH-POWER AMPLIFIER

## TECHNICAL FIELD

## 【0001】

10 The present invention relates to a high-power amplifier for amplifying an input signal to be output.

## BACKGROUND ART

## 【0002】

15 Generally, a high-power amplifier has a characteristic of increasing its output power with an increase in its input power, and of saturating at a certain level of the output power.

The efficiency of the high-power amplifier has a characteristic of increasing near the saturation and reducing at low output power.

20 Therefore the high-power amplifier has a problem of reducing its efficiency at the low output power.

## 【0003】

25 A mobile phone that adopts a communication scheme such as W-CDMA and N-CDMA controls its output power in accordance with the distance between the mobile phone and a base station and with radio wave conditions. The mobile phone, however, is more likely to carry out its transmission at the output power 10-15 dB less than the maximum output power.

30 Thus, it is necessary for the high-power amplifier used by the mobile phone to increase its efficiency (to reduce power

consumption) not only at the maximum output, but also at the output power 10-15 dB less than the maximum output to increase talk time.

【0004】

5       A conventional high-power amplifier makes a contrivance to increase the efficiency at the low output power by a design for decreasing an idle current.

          However, since it is insufficient, a high-power amplifier is proposed which tries to increase the efficiency at the low  
10       output power by controlling the drain voltage or collector voltage of an amplifying element in response to the output power (see Non-patent Document 1, for example).

          The following is the details.

【0005】

15       A signal input from an input terminal is supplied to an amplifying element via an input matching circuit composed of a DC-cut capacitor, capacitor and inductor, and is amplified. The signal output from the amplifying element is output from an output terminal via an output matching circuit composed of  
20       a DC-cut capacitor, capacitor and inductor.

          At the low output power, the efficiency of the high-power amplifier is increased by reducing the voltage output from a DC-DC converter by varying the value of a variable resistor.

【0006】

25       Non-patent Document 1: T. B. Nishimura, N. Iwata, and G. Hau, "IEEE MTT-S Symp. Digest", 1999, pp. 1091-1094.

【0007】

          With the foregoing configuration, the conventional high-power amplifier can improve the efficiency at the low output  
30       power to some extent by reducing the voltage output from the

DC-DC converter by varying the value of the variable resistor. However, since the DC-DC converter is bulky, it offers a problem of being difficult to miniaturize the high-power amplifier, and of increasing its cost. In addition, the efficiency of the DC-DC  
5 converter itself reduces the overall efficiency, offering a problem of impairing the efficiency at the low output power.

【0008】

The present invention is implemented to solve the foregoing problems. Therefore it is an object of the present invention  
10 to provide a high-power amplifier capable of increasing the efficiency at the low output power without increasing the cost or size.

#### DISCLOSURE OF THE INVENTION

15 【0009】

A high-power amplifier in accordance with the present invention changes the matching condition of a matching circuit connected between a final stage amplifying element and an output  
20 terminal in response to the output power of the amplifying element.

【0010】

Thus, it offers an advantage of being able to increase the efficiency at low output power without increasing its cost or  
25 size.

#### BRIEF DESCRIPTION OF THE DRAWINGS

【0011】

FIG. 1 is a block diagram showing a configuration of the high-power amplifier of an embodiment 1 in accordance with the  
30 present invention;

FIG. 2 is a circuit diagram showing an internal configuration of an output matching circuit of the high-power amplifier of the embodiment 1 in accordance with the present invention;

5        FIG. 3 is a chart illustrating variations in the optimum output load impedance of the final stage amplifying element due to the output power;

FIG. 4 is a table illustrating efficiency and ACPR (Adjacent Channel leakage Power Ratio) in the case of the optimum  
10 impedance;

FIG. 5 is a circuit diagram showing an internal configuration of the output matching circuit of the high-power amplifier of an embodiment 2 in accordance with the present invention;

15        FIG. 6 is a circuit diagram showing an internal configuration of the output matching circuit of the high-power amplifier of an embodiment 3 in accordance with the present invention;

FIG. 7 is a circuit diagram showing an internal  
20 configuration of a switch of the high-power amplifier of an embodiment 4 in accordance with the present invention;

FIG. 8 is a circuit diagram showing an internal configuration of the switch of the high-power amplifier of an embodiment 5 in accordance with the present invention;

25        FIG. 9 is a diagram illustrating calculation results of circuit voltages;

FIG. 10 is a circuit diagram showing an internal configuration of the switch of the high-power amplifier of an embodiment 6 in accordance with the present invention;

30        FIG. 11 is a block diagram showing a configuration of the

high-power amplifier of an embodiment 7 in accordance with the present invention;

FIG. 12 is a block diagram showing a configuration of the high-power amplifier of an embodiment 8 in accordance with the present invention;

FIG. 13 is a block diagram showing a configuration of the high-power amplifier of an embodiment 9 in accordance with the present invention;

FIG. 14 is a circuit diagram showing an internal configuration of an input matching circuit;

FIG. 15 is a circuit diagram showing an internal configuration of the input matching circuit;

FIG. 16 is a circuit diagram showing an internal configuration of the input matching circuit;

FIG. 17 is a diagram illustrating fluctuations in the pass phase characteristics of the high-power amplifier when reducing an idle collector current by decreasing a base voltage;

FIG. 18 is a diagram illustrating fluctuations in the pass phase characteristics of the high-power amplifier when reducing the idle collector current by decreasing the base voltage;

FIG. 19 is a diagram illustrating fluctuations in the pass phase characteristics of the high-power amplifier when reducing the idle collector current by decreasing the base voltage;

FIG. 20 is a diagram illustrating fluctuations in the pass phase of a two-stage HBT high-power amplifier when turning the switch on and off with varying the ratio between  $C_{on}$  and  $C_{off}$ ; and

FIG. 21 is a diagram illustrating fluctuations in the pass phase of the two-stage HBT high-power amplifier when turning the switch on and off with varying the ratio between  $C_{on}$  and

Coff.

## BEST MODE FOR CARRYING OUT THE INVENTION

### 【0012】

5       The best mode for carrying out the invention will now be described with reference to the accompanying drawings to explain the present invention in more detail.

#### EMBODIMENT 1

FIG. 1 is a block diagram showing a configuration of a  
10 high-power amplifier of an embodiment 1 in accordance with the present invention.

### 【0013】

In FIG. 1, an input terminal 1 is a terminal of the high-power amplifier for inputting an input signal. An input  
15 matching circuit 2, which is connected between the input terminal 1 and an amplifying element 3, tries to make matching between the input terminal 1 and amplifying element 3.

Each amplifying element 3, which is composed of such a device as an FET, HEMT, HBT and BJT, amplifies the input signal  
20 and outputs.

Each interstage matching circuit 4 is connected between two amplifying elements 3 to make matching between them.

### 【0014】

An output matching circuit 5 is connected between the final  
25 stage amplifying element 3 and an output terminal 8 to make matching between them.

A collector bias feed circuit 6, which is placed in the output matching circuit 5, supplies bias to the collector (or drain) of the final stage amplifying element 3.

30       A switching-function-attached matching circuit 7, which

is placed in the output matching circuit 5, changes matching conditions of the output matching circuit 5 under the control of a control circuit 11. The switching-function-attached matching circuit 7 constitutes a matching condition changing means.

5       【0015】

A base bias circuit 9 supplies a base bias (or gate bias) voltage to the base (or gate) of each of the multistage amplifying elements 3.

10       A collector bias circuit 10 supplies a collector bias (or drain bias) voltage to the collector (or drain) of each of the amplifying elements 3 except for the final stage amplifying element 3. In addition, it supplies a collector bias (or drain bias) voltage to the collector (or drain) of the final stage  
15       amplifying element 3 via the collector bias feed circuit 6.

The control circuit 11 controls the switching-function-attached matching circuit 7 in such a manner as to increase the imaginary part of the output load impedance of the final stage amplifying element 3 when the output power of the  
20       amplifying element 3 reduces.

      【0016】

FIG. 2 is a circuit diagram showing an internal configuration of the output matching circuit 5. In FIG. 2, an input terminal 21 is connected to the output terminal of the  
25       final stage amplifying element 3, a collector bias terminal 22 is connected to the collector bias circuit 10, and a control terminal 23 is connected to the control circuit 11.

A bypass capacitor 24 of the bias feed circuit 6 has its first terminal connected to the collector bias terminal 22 and  
30       its second terminal connected to a ground.

A quarter-wave line 25 of the bias feed circuit 6 has its first terminal connected to the collector bias terminal 22, and its second terminal connected to the input terminal 21.

【0017】

5       A series circuit of a DC-cut capacitor 26 and switch 27 constitutes a first impedance circuit, and the switch 27 is turned on and off under the control of the control circuit 11.

10       A series circuit of a capacitor 28 and inductor 29 constitutes a second impedance circuit that is connected in parallel with the first impedance circuit.

An inductor 30 and capacitor 31 are connected in series with the output terminal 8. Each of capacitors 32 and 33 has its first terminal connected to the inductor 30, and its second terminal connected to the ground.

15       【0018】

Next, the operation will be described.

The signal input through the input terminal 1 is supplied to the first stage amplifying element 3 via the input matching circuit 2.

20       Receiving the input signal from the input matching circuit 2, the first stage amplifying element 3 amplifies the input signal, and supplies the amplified signal to the next stage amplifying element 3 via the interstage matching circuit 4.

【0019】

25       Receiving the signal from the previous stage amplifying element 3 via the interstage matching circuit 4, each of the amplifying elements 3 from next stage to the final stage amplifies the signal in the same manner as the first stage amplifying element 3, and outputs it.

30       The signal output from the final stage amplifying element

3 is output from the output terminal 8 via the output matching circuit 5.

【0020】

FIG. 3 illustrates the calculation results of the optimum output load impedance of the final stage amplifying element 3 due to the variations in the output power. Here, the optimum output load impedance refers to the output load impedance that will maximize the efficiency within the range satisfying a standardized distortion specification.

The amplifying elements 3 used for the calculation are an InGaP HBT (32 fingers with  $4 \times 20 \mu\text{m}^2$  per finger); the bias conditions is  $V_c = 3.5 \text{ V}$ ; the idle collector current is  $I_{cq} = 18 \text{ mA}$ ; the frequency is  $1.95 \text{ GHz}$ ; and modulation waves for W-CDMA mobile phone terminals are used.

【0021】

In the example of FIG. 3, an optimum output load impedance is an impedance that will give a maximum efficiency at  $\text{ACPR} < -38 \text{ dBc}$  at each output against the W-CDMA modulation waves. The term ACPR (Adjacent Channel leakage Power Ratio) refers to distortion characteristics.

In addition, the optimum output load impedance moves toward the direction that increases the imaginary part of the impedance as the output power is reduced with respect to the maximum output  $25 \text{ dBm}$ .

【0022】

FIG. 4 illustrates the calculation results of the efficiency and ACPR values in the case of the optimum output load impedance of FIG. 3 at each output power.

$I_{cq} \text{ Const.}$  in FIG. 4 refers to the calculation results in the condition where the base voltage is kept constant ( $I_{cq}$  is

constant). In contrast,  $I_{cq}$  Control refers to the results when the idle collector current  $I_{cq}$  is controlled to reduced values within the range that meets the condition of  $ACPR < -38$  dBc.

【0023】

5           For example, when the output power is reduced to 11 dBm by 14 dB in the condition where the optimum output load impedance at the output power of 25 dBm is maintained, the efficiency becomes 9%.

          Therefore it is found from FIG. 4 that when the output power  
10 is reduced, the efficiency can be improved from 9% to 18% by implementing the optimum impedance at the output power 11 dBm by increasing the imaginary part of the output load impedance (see FIG. 3).

【0024】

15           Thus, in the present embodiment 1, the control circuit 11 observes the output power of the amplifying element 3, and controls, when the output power reduces, the switching-function-attached matching circuit 7 in such a manner as to increase the imaginary part of the output load impedance of the  
20 final stage amplifying element 3. Here, although it is assumed that the output power of the final stage amplifying element 3 is observed, it is also possible to observe the output power of other amplifying element 3.

          The following is the details.

25   【0025】

          First, the collector bias feed circuit 6 composed of the bypass capacitor 24 and quarter-wave line 25 is connected to the input terminal 21 of the output matching circuit 5. However, at the used frequency, since the collector bias feed circuit  
30 6 makes open the impedance causing a short circuit at the bypass

capacitor 24 by the quarter-wave line 25, the collector bias feed circuit 6 has no effect on the output load impedance of the final stage amplifying element 3.

Accordingly, the output load impedance of the final stage  
5 amplifying element 3 is determined by the switching-function-attached matching circuit 7.

**【0026】**

The switching-function-attached matching circuit 7 has a circuit including the series circuit of the DC-cut capacitor  
10 26 and switch 27 and the series circuit of the capacitor 28 and inductor 29, which series circuits are connected in parallel.

The control circuit 11 observes the output power of the amplifying element 3, and turns on the switch 27 of the switching-function-attached matching circuit 7 when the output  
15 power is greater than predetermined power, thereby causing the output signal of the final stage amplifying element 3 to pass through the DC-cut capacitor 26. In this case, the output signal scarcely flows through the capacitor 28 and inductor 29.

In contrast, when the output power of the amplifying element  
20 3 is less than the predetermined power, the control circuit 11 turns off the switch 27 of the switching-function-attached matching circuit 7 so that the output signal of the final stage amplifying element 3 passes through the capacitor 28 and inductor 29.

25 **【0027】**

In this way, when the output power of the amplifying element 3 reduces, the imaginary part of the output load impedance of the amplifying element 3 is increased as compared when the output power is large.

30 Therefore when the capacitors 26, 31, 32 and 33 and inductor

30 are designed in such a manner as to implement the optimum load impedance at the maximum output in the case where the switch 27 is made on, the imaginary component can be increased by the difference between the reactance component of the inductor 29 and that of the DC-cut capacitor 26 in the case where the switch 27 is made off. Here, the value of the inductor 29 is set at a value that will implement the optimum load impedance at the low output power when the switch 27 is turned off.

【0028】

10 As is clear from the foregoing description, the present embodiment 1 is configured in such a manner as to change the matching conditions of the output matching circuit 5 connected between the final stage amplifying element 3 and output terminal 8 in response to the output power of the amplifying element 3. 15 Thus, the present embodiment 1 offers an advantage of being able to greatly increase the efficiency at the low output power without reducing the efficiency at the maximum output. In addition, since it can obviate the need for the DC-DC converter, it offers an advantage of being able to prevent an increase in size and cost. 20

【0029】

Furthermore, the present embodiment 1 is configured in such a manner as to turn on the switch 27 of the switching-function-attached matching circuit 7 when the output power of the amplifying element 3 is greater than the predetermined power, 25 and to turn off the switch 27 of the switching-function-attached matching circuit 7 when the output power of the amplifying element 3 is less than the predetermined power. Thus, the present embodiment 1 offers an advantage of being able to 30 implement the optimum load impedance easily both at the maximum

and low output power.

【0030】

Incidentally, when the switch 27 of the switching-function-attached matching circuit 7 is composed of a diode or transistor, the distortion characteristics are usually worse when the switch 27 is turned off. The present embodiment 1 can control the distortion characteristics caused by the switch 27, because the low output power occurs at the off timing of the switch in which the distortion characteristics are severer.

【0031】

#### EMBODIMENT 2

FIG. 5 is a circuit diagram showing an internal configuration of the output matching circuit 5 of the high-power amplifier of an embodiment 2 in accordance with the present invention.

It differs from the output matching circuit 5 of FIG. 2 in that the capacitor 32 of the switching-function-attached matching circuit 7 is moved toward the final stage amplifying element 3 side. Thus, the capacitor 32 is connected in parallel with the collector bias feed circuit 6. Here, a line can be interposed between the collector bias feed circuit 6 and the capacitor 32.

【0032】

Next, the operation will be described.

The collector bias feed circuit 6 composed of the bypass capacitor 24 and quarter-wave line 25 is connected to the input terminal 21 of the output matching circuit 5. However, since the collector bias feed circuit 6 makes open the impedance causing the short circuit at the bypass capacitor 24 at the used

frequency by the quarter-wave line 25, the collector bias feed circuit 6 has no effect on the output load impedance of the final stage amplifying element 3.

【0033】

5        In reality, however, it sometimes occurs that the quarter-wave line 25 cannot be achieved up to the full length of the quarter wave, and is shorter than the quarter wave. In this case, the collector bias feed circuit 6 has some effect on the output load impedance of the final stage amplifying  
10    element 3.

【0034】

      In the present embodiment 2, the capacitor 32 of the switching-function-attached matching circuit 7 is moved toward the final stage amplifying element 3, and is connected in  
15    parallel with the collector bias feed circuit 6. Thus, even if the quarter-wave line 25 is shorter than the quarter wave, the present embodiment 2 can cancel out the parallel inductance component caused by being shorter than the quarter wave.

      Therefore the output load impedance of the final stage  
20    amplifying element 3 is made free from the effect of the collector bias feed circuit 6, to which the capacitor 32 of the switching-function-attached matching circuit 7 is connected.

【0035】

      In this case, the output load impedance of the final stage  
25    amplifying element 3 is determined by the switching-function-attached matching circuit 7 without including the capacitor 32 moved toward the final stage amplifying element 3 side.

      Accordingly, when the capacitors 26, 31 and 33 and inductor  
30    30 are designed in such a manner as to implement the optimum

load impedance at the maximum output in the case where the switch 27 is made on, the imaginary component can be increased by the difference between the reactance component of the inductor 29 and that of the DC-cut capacitor 26 in the case where the switch 27 is made off. Here, the value of the inductor 29 is set at a value that will implement the optimum load impedance at the low output power when the switch 27 is turned off.

#### 【0036】

As is clear from the foregoing description, when the bias feed circuit 6 for supplying the bias to the collector of the final stage amplifying element 3 is connected to the input terminal 21 of the output matching circuit 5, the present embodiment 2 is configured in such a manner as to connect the capacitor 32 in parallel with the collector bias feed circuit 6. Thus, even if the quarter-wave line 25 of the collector bias feed circuit 6 cannot be achieved up to the full length of the quarter wave, the present embodiment 2 offers an advantage of being able to cancel out the parallel inductance component caused by being shorter than the quarter wave.

#### 【0037】

##### EMBODIMENT 3

FIG. 6 is a circuit diagram showing an internal configuration of the output matching circuit 5 of the high-power amplifier an embodiment 3 in accordance with the present invention.

In FIG. 6, since the same reference numerals designate the same or like portions to those of FIG. 5, their description will be omitted here.

#### 【0038】

A series circuit of a DC-cut capacitor 41 and switch 42 constitutes a first impedance circuit, and the switch 42 is turned on and off under the control of the control circuit 11.

A capacitor 43 constitutes a second impedance circuit that is connected in parallel with the first impedance circuit.

【0039】

Next, the operation will be described.

It sometimes occurs that the quarter-wave line 25 cannot be achieved up to the full length of the quarter wave. Thus, as in the foregoing embodiment 2, the capacitor 32 of the switching-function-attached matching circuit 7 is moved toward the final stage amplifying element 3 side to be connected in parallel with the collector bias feed circuit 6.

Therefore the output load impedance of the final stage amplifying element 3 is free from the effect of the collector bias feed circuit 6, to which the capacitor 32 of the switching-function-attached matching circuit 7 is connected.

【0040】

In this case, the output load impedance of the final stage amplifying element 3 is determined by the switching-function-attached matching circuit 7 without the capacitor 32 moved toward the final stage amplifying element 3 side.

【0041】

The control circuit 11 observes the output power of the amplifying element 3, and turns off the switch 42 of the switching-function-attached matching circuit 7 when the output power is greater than predetermined power, thereby causing the output signal of the final stage amplifying element 3 to pass through the capacitor 43.

In contrast, when the output power of the amplifying element

3 is less than the predetermined power, the control circuit 11 turns on the switch 42 of the switching-function-attached matching circuit 7 so that the output signal of the final stage amplifying element 3 passes through both the capacitor 41 and capacitor 43, thereby increasing the value of the series capacitors.

【0042】

In this way, when the output power of the amplifying element 3 reduces, the imaginary part of the output load impedance of the amplifying element 3 is increased as compared when the output power is large.

Therefore when the capacitors 31, 33 and 43 and inductor 30 are designed in such a manner as to implement the optimum load impedance at the maximum output in the case where the switch 42 is made off, the imaginary component of the output load impedance can be increased in the case where the switch 27 is made on. Here, the value of the capacitor 43 is set at a value that will implement the imaginary component of the difference between the optimum impedance at the maximum output and the optimum impedance at the low output power.

【0043】

As is clear from the foregoing description, the present embodiment 3 is configured in such a manner as to turn off the switch 42 of the switching-function-attached matching circuit 7 when the output power of the amplifying element 3 is greater than the predetermined power, and to turn on the switch 42 of the switching-function-attached matching circuit 7 when the output power of the amplifying element 3 is less than the predetermined power. Thus, the present embodiment 3 offers an advantage of being able to implement the optimum load impedance

easily at both the maximum and low output power.

In addition, since the present embodiment 3 can eliminate the inductor 29, it offers an advantage of being able to miniaturize the high-power amplifier.

5 Furthermore, the present embodiment 3 offers an advantage of being able to prevent the reduction in the efficiency at the maximum output, because the switch 42 of the switching-function-attached matching circuit 7 is made off when the output power of the amplifying element 3 is greater than the  
10 predetermined power.

#### 【0044】

#### EMBODIMENT 4

FIG. 7 is a circuit diagram showing an internal  
15 configuration of the switch 27 or 42 of the high-power amplifier of an embodiment 4 in accordance with the present invention.

In FIG. 7, a diode 53 such as a PIN diode, Schottky diode or PN diode is connected between an input terminal 51 and an output terminal 52.

#### 20 【0045】

A bias feed resistor 54 has its first terminal connected to the input terminal 51, and its second terminal connected to the ground.

A bias feed resistor 55 has its first terminal connected  
25 to the output terminal 52, and its second terminal connected to the control terminal 23.

#### 【0046】

Next, the operation will be described.

The switch 27 or 42 of the switching-function-attached  
30 matching circuit 7 is implemented by turning on and off the bias

of the diode 53. To feed the bias to the diode 53, it is possible to use the bias feed resistors 54 and 55, or bias feed inductors 56 as shown in FIG. 7.

【0047】

5 Using the bias feed resistors 54 and 55, however, can miniaturize the high-power amplifier in its entirety, because they can be formed on the same semiconductor substrate as the amplifying elements 3.

10 In addition, when the Schottky diode or PN diode is used as the diode 53, and a contrivance is made to construct the Schottky diode with using the source and drain electrodes of an FET in common, or the PN diode with using the emitter and collector of a BJT or HBT in common, the diode 53 can be easily formed on the same substrate as the amplifying elements 3,  
15 thereby being able to miniaturize the high-power amplifier in its entirety. The miniaturization can also bring about the cost reduction.

【0048】

To turn on the diode 53, the control circuit 11 applies  
20 a positive voltage to the control terminal 23.

In contrast, to turn off the diode 53, the control circuit 11 applies a zero or negative voltage to the control terminal 23.

25 When the signal input to the diode 53 is large, the distortion characteristics deteriorate, particularly when turning off the diode 53. In such a case, it is necessary to apply the negative voltage.

【0049】

When using the PIN diode as the diode 53, it is possible  
30 to turn on the diode 53 with a less diode current than when using

the Schottky diode or PN diode, thereby being able to reduce the current consumption of the diode 53. In this case, an advantage is offered of being able to increase the efficiency of the high-power amplifier in its entirety.

5

【0050】

#### EMBODIMENT 5

FIG. 8 is a circuit diagram showing an internal configuration of the switch 27 or 42 of the high-power amplifier of an embodiment 5 in accordance with the present invention.

In FIG. 8, since the same reference numerals designate the same or like portions to those of FIG. 7, their description will be omitted here.

【0051】

15 A power supply voltage application terminal 57 is supplied with a power supply voltage  $V_{cc}$ . A transistor 58 constitutes a transistor switch consisting of a BJT, HBT or FET, for example.

A resistor 59, whose resistance value is  $R_c$ , has its first terminal connected to the power supply voltage application terminal 57, and its second terminal connected to the collector of the transistor 58.

20 A resistor 60, whose resistance value is  $R_b$ , has its first terminal connected to the control terminal 23, and its second terminal connected to the base of the transistor 58.

25 【0052】

Next, the operation will be described.

The switch 27 or 42 of the switching-function-attached matching circuit 7 is implemented by turning on and off the bias of the diode 53.

30 To turn on the diode 53, the control circuit 11 applies

a positive voltage to the control terminal 23 as in the foregoing embodiment 4. However, to prevent the deterioration in the distortion characteristics at turning off the diode 53, it is necessary to apply a negative voltage.

5           However, considering a demand for carrying out everything by using positive voltages, the present embodiment 5 devises a method of preventing the deterioration in the distortion characteristics in the off state even if the control circuit 11 applies zero volt to the control terminal 23.

10           The following is the details.

**【0053】**

First, the power supply voltage application terminal 57 is always supplied with the positive power supply voltage  $V_{cc}$ .

15           When the control circuit 11 applies the control voltage  $V_{cont}$  of zero volt to the control terminal 23, the transistor 58 is turned off. Thus, no current flows through the transistor 58 so that the output side voltage  $V_{d-}$  of the transistor 58 agrees with the power supply voltage  $V_{cc}$ .

20           In addition, the input side voltage  $V_{d+}$  of the transistor 58 is placed at zero volt, because it is identical to the control voltage  $V_{cont}$ .

Accordingly the diode 53 is supplied with the negative voltage  $-V_{cc}$ .

**【0054】**

25           On the other hand, when the control circuit 11 supplies a positive control voltage  $V_{cont}$  (such as +2.5 V) to the control terminal 23, the transistor 58 is turned on and a current  $I_c$  flows through the transistor 58.

30           Accordingly, the output side voltage  $V_{d-}$  of the transistor 58 becomes the difference obtained by subtracting the voltage

drop by the resistor 59 from the power supply voltage  $V_{cc}$ , that is,  $V_{cc} - R_c \times I_c$ . When the resistance value  $R_c$  of the resistor 59 is large, the output side  $V_{d-}$  of the transistor 58 becomes about 0.5 V, which is the knee voltage of the transistor 58.

5     **【0055】**

On the other hand, the input side voltage  $V_{d+}$  of the transistor 58 is identical to the control voltage  $V_{cont}$  itself, and is +2.5 V, for example.

Accordingly, the diode 53 is supplied with a positive  
10 voltage of +2.0 V.

**【0056】**

FIG. 9 illustrates the calculation results of the circuit voltages, and shows that it is possible to supply the diode 53 with the positive polarity and negative polarity voltages using  
15 only positive voltage.

Thus, the present embodiment 5 can operate the diode 53 at low distortion using only positive voltage for the control.

In addition, since the present embodiment 5 is configured using only the resistors and transistor, it can be constructed  
20 on the same substrate as the amplifying elements 3, thereby being able to miniaturize the high-power amplifier.

**【0057】**

#### EMBODIMENT 6

25     FIG. 10 is a circuit diagram showing an internal configuration of the switch of the high-power amplifier of an embodiment 6 in accordance with the present invention.

In FIG. 10, since the same reference numerals designate the same or like portions to those of FIG. 7, their description  
30 will be omitted here.

【0058】

A transistor 71, which is a transistor such as a BJT, HBT or FET, is connected between the input terminal 51 and output terminal 52.

5 A resistor 72 has its first terminal connected to the base of the transistor 71, and its second terminal connected to the control terminal 23.

【0059】

Next, the operation will be described.

10 The control circuit 11 controls the voltage to be applied to the control terminal 23. Thus, it can turn on and off the transistor 71.

Thus, the transistor 71 operates as a switch. In this case, the pass loss due to the control terminal 23 side impedance can  
15 be made small because the transistor 71 can provide sufficient isolation between the path through which the control signal input via the control terminal 23 passes and the path through which the signal input via the input terminal 51 passes.

【0060】

20 Therefore the present embodiment 6 can achieve higher efficiency than the foregoing embodiment 3. At the same time, when a mechanical switch such as a MEMS switch is used in place of the transistor 71, the efficiency of the high-power amplifier can be further improved because of the small pass loss of the  
25 MEMS switch.

【0061】

EMBODIMENT 7

FIG. 11 is a block diagram showing a configuration of the  
30 high-power amplifier of an embodiment 7 in accordance with the

present invention.

In FIG. 11, since the same reference numerals designate the same or like portions to those of FIG. 1, their description will be omitted here.

5     **【0062】**

A base bias circuit 12 controls, under the control of the control circuit 13, the base bias (or gate bias) voltage to be supplied to the base (or gate) of each amplifying element 3. Here, the base bias circuit 12 constitutes a voltage control  
10 means.

As the control circuit 11 of FIG. 1, the control circuit 13 controls the switching-function-attached matching circuit 7 in such a manner as to increase the imaginary part of the output load impedance of the final stage amplifying element 3 when the  
15 output power of the amplifying element 3 reduces, and controls the base bias circuit 12 in such a manner as to reduce the idle current of each amplifying element 3 when the output power of the amplifying element 3 reduces.

**【0063】**

20     Next, the operation will be described.

The present embodiment 7 differs from the foregoing embodiment 1 in that when the output power of the amplifying element 3 reduces, the present embodiment 7 not only controls the switching-function-attached matching circuit 7 in such a  
25 manner as to increase the imaginary part of the output load impedance of the final stage amplifying element 3, but also controls the base bias circuit 12 in such a manner as to reduce the idle current of the amplifying elements 3.

The different point will be described in more detail.

30     **【0064】**

FIG. 4 shows the calculation results of the  $I_{cq}$  Control when the idle collector current  $I_{cq}$  is reduced in the range that satisfies  $ACPR < -38$  dBc. Thus, when switching the output load impedance between the maximum output and the low output power as illustrated in FIG. 3, the efficiency at the low output power can be further increased by reducing the idle current of the collector at the low output power by controlling the base bias voltage of the amplifying elements 3 as shown in FIG. 4.

【0065】

In view of this, in the present embodiment 7, the control circuit 13 observes the output power of the amplifying element 3, and supplies the base bias circuit 12 with the control signal instructing to reduce the idle current of the amplifying elements 3 when the output power becomes less than the predetermined power.

Receiving the control signal instructing to reduce the idle current from the control circuit 13, the base bias circuit 12 increases the base bias voltages supplied to the bases of the amplifying elements 3, thereby reducing the idle current of the amplifying elements 3.

【0066】

As is clear from the foregoing description, the present embodiment 7 is configured in such a manner as to control the base bias voltages of the amplifying elements 3 in such a fashion as to reduce the idle current of the amplifying elements 3 when the output power of the amplifying element 3 reduces. Thus, the present embodiment 7 offers an advantage of being able to increase the efficiency at the low output power further than the foregoing embodiment 1.

【0067】

EMBODIMENT 8

FIG. 12 is a block diagram showing a configuration of the high-power amplifier of an embodiment 8 in accordance with the present invention.

In FIG. 12, since the same reference numerals designate the same or like portions to those of FIG. 11, their description will be omitted here.

【0068】

10 A collector bias circuit 14 controls the collector bias (or drain bias) voltage supplied to the collector (or drain) of each amplifying element 3 under the control of a control circuit 15. The collector bias circuit 14 constitutes a voltage control means.

15 Just as the control circuit 13 of FIG. 11, when the output power of the amplifying element 3 reduces, the control circuit 15 controls the switching-function-attached matching circuit 7 in such a manner as to increase the imaginary part of the output load impedance of the final stage amplifying element 3, and the  
20 base bias circuit 12 in such a manner as to reduce the idle current of the amplifying elements 3. In addition, the control circuit 15 controls the collector bias circuit 14 when the output power of the amplifying element 3 reduces.

【0069】

25 Next, the operation will be described.

The present embodiment 8 differs from the foregoing embodiment 7 in that when the output power of the amplifying element 3 reduces, the present embodiment 8 not only controls the base bias circuit 12 in such a manner as to reduce the idle  
30 current of the amplifying elements 3, but also reduces the

collector bias voltage of the amplifying elements 3.

The different point will be described in more detail below.

【0070】

The efficiency at the low output power can be further  
5 increased without reducing the efficiency at the maximum output  
by reducing the collector bias voltage of the amplifying elements  
3 within the range in which ACPR indicating the distortion  
characteristics satisfies the standards.

【0071】

10 In view of this, in the present embodiment 8, the control  
circuit 15 observes the output power of the amplifying element  
3, and supplies, when the output power falls below the  
predetermined power, the collector bias circuit 14 with the  
control signal instructing to reduce the collector bias voltage  
15 of the amplifying elements 3.

Receiving the control signal instructing to reduce the  
collector bias voltage of the amplifying elements 3 from the  
control circuit 15, the collector bias circuit 14 reduces the  
collector bias voltage supplied to the collectors of the  
20 amplifying elements 3.

【0072】

As is clear from the foregoing description, the present  
embodiment 8 is configured in such a manner as to reduce the  
collector bias voltage of the amplifying elements 3 when the  
25 output power of the amplifying element 3 reduces. Thus, the  
present embodiment 8 offers an advantage of being able to  
increase the efficiency at the low output power further than  
the foregoing embodiment 7.

【0073】

30 Although the present embodiment 8 is described by way of

example in which the collector bias circuit 14 controls the collector bias voltage of the amplifying elements 3, it is also possible to use a DC-DC converter or Class S modulator in place of the collector bias circuit 14.

5

**【0074】**

## EMBODIMENT 9

FIG. 13 is a block diagram showing a configuration of the high-power amplifier of an embodiment 9 in accordance with the present invention.

10

In FIG. 13, since the same reference numerals designate the same or like portions to those of FIG. 12, their description will be omitted here.

**【0075】**

A phase adjusting circuit 16 adjusts, under the control of the control circuit 17, the pass phase of the input signal in such a manner as to reduce the fluctuations in the pass phase when the matching conditions of the output matching circuit 5 are changed.

15

Although the phase adjusting circuit 16 is placed in the input matching circuit 2 in the example of FIG. 13, this is not essential. For example, even if the phase adjusting circuit 16 is placed in the interstage matching circuit 4, it can adjust the pass phase of the input signal in such a manner as to reduce the fluctuations in the pass phase at the changes in the matching conditions of the output matching circuit 5.

20

25

**【0076】**

The control circuit 17 controls not only the switching-function-attached matching circuit 7, base bias circuit 12 and collector bias circuit 14 just as the control

30

circuit 15 of FIG. 12, but also the phase adjusting circuit 16.

【0077】

FIG. 14 is a circuit diagram showing an internal configuration of the input matching circuit 2. In FIG. 14, an output terminal 81 is connected to the first stage amplifying element 3, and a control terminal 82 is connected to the control circuit 17.

A capacitor 83 has its first terminal connected to the input terminal 1, and its second terminal connected to the phase adjusting circuit 16.

An inductor 84 has its first terminal connected to the second terminal of the capacitor 83, and its second terminal connected to the ground.

【0078】

A switch 85 undergoes the on and off control by the control circuit 17. A capacitor 86, which is connected in series with the switch 85, has a capacitance value of  $C_{on}$ .

A capacitor 87, which is connected in parallel with the series circuit composed of the switch 85 and capacitor 86, has a capacitance value of  $C_{off}$ .

【0079】

Next, the operation will be described.

The present embodiment 9 differs from the foregoing embodiment 8 in that the input matching circuit 2 includes the phase adjusting circuit 16.

The different point will be described in more detail below.

【0080】

FIG. 17 to FIG. 19 each illustrates calculation results of the fluctuations in the pass phase characteristics of the high-power amplifier when the idle collector current is reduced

by dropping the base voltage when switching the output matching circuit 5 at the low output power in a two-stage amplifier using an HBT.

Here, the calculation is carried out assuming that the switch 27 of FIG. 5 is used as the circuit for switching the impedance in the output matching circuit 5.

【0081】

In particular, FIG. 17 illustrates the calculation results of the pass phase characteristics at the maximum output condition, that is, when the switch 27 is in the on state and before the bias conditions are changed.

FIG. 18 illustrates the calculation results when the switch 27 is turned off at the low output power.

FIG. 19 illustrates the calculation results when the idle collector current is reduced by varying the bias conditions in addition to the turning off of the switch 27.

【0082】

As is clear from FIG. 17 to FIG. 19, the pass phase characteristics at 1.95 GHz vary by +35.5 degrees from -108.8 degrees to -73.3 degrees by switching the output matching circuit 5.

In addition, it is found that the pass phase characteristics vary by +17.9 degrees from -108.8 degrees to -90.9 degrees by varying both the output matching circuit 5 and bias conditions simultaneously.

【0083】

When the pass phase of the signal changes greatly in communications equipment, in particular in a receiver utilizing a synchronous detection method, it is likely that synchronization error occurs and the communication is

interrupted. Accordingly, the fluctuations in the pass phase characteristics must be kept small, and hence the phase fluctuations must be reduced in the high-power amplifier as well.

Thus, the present embodiment 9 has the phase adjusting circuit 16 placed in the input matching circuit 2 to reduce the fluctuations in the pass phase.

**【0084】**

The control circuit 17 observes the output power of the amplifying element 3, and turns on the switch 85 of the phase adjusting circuit 16 when the output power is greater than the predetermined power (when the switch 27 of FIG. 5 is in the on state).

In contrast, when the output power of the amplifying element 3 is less than the predetermined power (when the switch 27 of FIG. 5 is in the off state), the control circuit 17 turns off the switch 85 of the phase adjusting circuit 16.

**【0085】**

Thus, the input matching of the high-power amplifier is carried out by the capacitors 83, 86 and 87 and inductor 84 at the high output in which the switch 85 of the phase adjusting circuit 16 is in the on state.

In contrast, at the low output power in which the switch 85 of the phase adjusting circuit 16 is in the off state, the input matching is carried out by the capacitors 83 and 87 and inductor 84.

**【0086】**

Therefore at the high output in which the switch 85 of the phase adjusting circuit 16 is in the on state, the total capacitance value  $C_{on} + C_{off}$  of the capacitors 86 and 87 is set in such a manner as to achieve the input matching in the state

of the maximum output.

In addition, the ratio between the capacitance value  $C_{on}$  of the capacitor 86 and the capacitance value  $C_{off}$  of the capacitor 87 is determined to cancel out the pass phase  
 5 fluctuations caused by the switching of the output matching or of the bias conditions at the low output power.

【0087】

FIG. 20 and FIG. 21 illustrate calculation results of the pass phase fluctuations in the two-stage HBT high-power  
 10 amplifier when the switch 85 is turned on and off in the case where the ratio between  $C_{on}$  and  $C_{off}$  varies under the condition in which  $C_{on} + C_{off} = 2.3 \text{ pF}$  is kept constant.

In particular, FIG. 20 illustrates the calculation results when the switch 85 is in the on state; and FIG. 21 illustrates  
 15 the calculation results when the switch 85 is in the off state.

FIG. 20 and FIG. 21 each illustrate examples in which the combinations of  $C_{on}/C_{off}$  are  $0.2 \text{ pF}/2.1 \text{ pF}$ ,  $0.4 \text{ pF}/1.9 \text{ pF}$ ,  $0.6 \text{ pF}/1.7 \text{ pF}$ ,  $0.8 \text{ pF}/1.5 \text{ pF}$ ,  $1.0 \text{ pF}/1.3 \text{ pF}$  and  $1.2 \text{ pF}/1.1 \text{ pF}$ .

【0088】

20 It is found from FIG. 20 that the pass phase little varies when the switch 85 is in the on state because  $C_{on} + C_{off} = 2.3 \text{ pF}$  is constant.

In contrast, it is found from FIG. 21 that the pass phase fluctuations in the negative direction increase as the ratio  
 25 of the  $C_{on}$  increases when the switch 85 is in the off state.

【0089】

Thus, it is found that the phase varies in the direction opposite to the direction resulting from the output matching switching and bias condition switching illustrated in FIG. 17  
 30 to FIG. 19.

In view of this, setting the values of Con and Coff appropriately makes it possible to reduce the pass phase fluctuations with maintaining the input matching.

【0090】

5       As is clear from the foregoing description, the present embodiment 9 has the phase adjusting circuit 16 for adjusting the pass phase of the input signal in the input matching circuit 2 of the amplifying element 3 in order to reduce the pass phase fluctuations at the time when the matching conditions of the  
10       output matching circuit 5 are changed. Thus, the present embodiment 9 offers an advantage of being able to reduce the pass phase fluctuations even when the matching conditions of the output matching circuit 5 are changed.

【0091】

15       Although the present embodiment 9 is described by way of example in which the phase adjusting circuit 16 is placed in the input matching circuit 2, the phase adjusting circuit 16 can also be placed in the interstage matching circuit 4.

      In this case, since the phase adjusting circuit 16 is placed  
20       neither on the input side or output side of the high-power amplifier, deterioration in the noise characteristics or efficiency characteristics due to the loss of the phase adjusting circuit 16 can be eliminated almost completely. Accordingly, the present embodiment 9 can reduce the pass phase fluctuations  
25       with maintaining the noise characteristics or efficiency.

【0092】

      Although the present embodiment 9 is described by way of example in which the phase adjusting circuit 16 includes the switch 85, this is not essential. For example, as shown FIG.  
30       15, the phase adjusting circuit 16 can include a diode 91 such

as a PIN diode, Schottky diode and PN diode. In this case, although the diode 91 is connected to the control terminal 82 via a bias feed resistor 92, a bias feed inductor 93 can be connected in place of the bias feed resistor 92.

5    **【0093】**

Utilizing the PIN diode as in FIG. 15 enables a reduction in the current consumption in the on state of the diode 91, thereby being able to increase the efficiency.

In addition, when employing a Schottky diode or PN diode, 10 the diode 91 can be implemented by using the source and drain terminals of an FET in common, or by using the emitter and collector terminals of the HBT in common.

As for the Schottky diode or PN diode, they can be formed on the same semiconductor substrate as the amplifying element 15 used for the high-power amplifier together with the capacitors and resistors. Accordingly, they can be integrated into an MMIC, enabling the miniaturization of the high-power amplifier.

**【0094】**

Alternatively, as shown in FIG. 16, the phase adjusting 20 circuit 16 can include a transistor 94 such as a BJT, HBT and FET.

When employing the transistor 94 such as the BJT, HBT and FET as shown in FIG. 16, they can be formed on the same semiconductor substrate as the amplifying element 3 used for 25 the high-power amplifier together with the capacitors and resistors. Accordingly, they can be integrated into an MMIC, enabling the miniaturization of the high-power amplifier.

In addition, since the transistor 94 isolates the signal line from the control terminal 82, it can implement a low loss 30 switch, which enables the reduction in the loss of the phase

adjusting circuit 16, and the low noise, high efficiency characteristics.

【0095】

Incidentally, a mechanical switch such as a MEMS switch  
5 can be used as the switch 85. Employing the MEMS switch makes  
it possible to implement the low noise, high efficiency  
characteristics because the MEMS switch has low loss  
characteristics and hence reduces the loss of the phase adjusting  
circuit 16.

10

INDUSTRIAL APPLICABILITY

【0096】

As described above, the high-power amplifier in accordance  
with the present invention is suitable for mobile phones and  
15 the like requiring improved efficiency even when they transmit  
at the low output power 10-15 dB less than the maximum output  
power.